IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A semiconductor device, comprising:

a data memory ~~which stores~~configured to store data and a test pattern;

an error checking and correcting unit (ECC unit) configured to output the test pattern to the data memory, and to generate, from a Hamming matrix which meets a given condition and a transposed matrix of the test pattern, an error checking and correcting code (ECC code) as generated code data corresponding to the stored data and configured for use in checking bit errors of all cells in the data memory; and

a code memory configured to store the ECC code.

~~a code memory which stores an error checking and correcting code (ECC code) corresponding to the data; and~~

~~an error checking and correcting unit (ECC unit) which outputs, to the data memory as the data, a test pattern required to test the data memory, and which generates, from the test pattern, code information having an error checking function, and outputs the code information to the code memory as the error checking and correcting code.~~

Claim 2 (Currently Amended): The semiconductor device according to claim 1, the ECC unit ~~further~~ comprising:

a test unit configured to generate the test pattern and simultaneously test bit errors of all cells in the data memory and bit errors of all cells in the code memory by reading the test pattern written in the data memory and the code data written in the code memory.

~~a test unit which simultaneously tests the data memory and the code memory by reading the test pattern written in the data memory and the code information written in the code memory.~~

Claim 3 (Canceled).

Claim 4 (Currently Amended): The semiconductor device according to claim 1, wherein the given condition is that a sum of row components of the Hamming matrix is odd.

~~wherein the ECC unit generates the code information using a Hamming matrix configured so that a sum of row components of the matrix is odd.~~

Claim 5 (Currently Amended): The semiconductor device according to claim 2, wherein the given condition is that a sum of row components of the Hamming matrix is odd.

~~wherein the ECC unit generates the code information using a Hamming matrix configured so that a sum of row components of the matrix is odd.~~

Claim 6 (Currently Amended): The semiconductor device according to claim 1,

wherein the given condition is that all bits of the generated code data are "1"s, when all bits of the test pattern are "1"s.

~~wherein if all bits of the test pattern are "1"s, the ECC unit generates the code information so that all bits of code information generated from the test pattern are "1"s.~~

Claim 7 (Currently Amended): The semiconductor device according to claim 2,

wherein the given condition is that all bits of the generated code data are "1"s, when all bits of the test pattern are "1"s.

~~wherein if all bits of the test pattern are "1"s, the ECC unit generates the code information so that all bits of code information generated from the test pattern are "1"s.~~

Claim 8 (Currently Amended): The semiconductor device according to claim 1,

wherein the given condition is that all bits of the generated code data change from "0" to "1" or "1" to "0" in accordance with the test pattern.

~~wherein the ECC unit generates the code information so that all the bits of the code information change from "0" to "1" or "1" to "0" in accordance with the inputting of the test pattern.~~

Claim 9 (Currently Amended): The semiconductor device according to claim 2,

wherein the given condition is that all bits of the generated code data change from "0" to "1" or "1" to "0" in accordance with the test pattern.

~~wherein the ECC unit generates the code information so that all the bits of the code information change from "0" to "1" or "1" to "0" in accordance with the inputting of the test pattern.~~

Claim 10 (Currently Amended): The semiconductor device according to claim 1,

wherein the given condition is that an arbitrary N (N is a natural number equal to or greater than 2) bits having a common address in the test pattern and in the generated code data cover all patterns of N-bit combinations in accordance with the test pattern.

~~wherein the ECC unit generates the code information so that an arbitrary N (N is a natural number equal to or greater than 2) bits of the same address in the test pattern and in the code information generated from the test pattern cover all patterns of N-bit combinations in accordance with the inputting of the test pattern.~~

Claim 11 (Currently Amended): The semiconductor device according to claim 2,

wherein the given condition is that an arbitrary N (N is a natural number equal to or greater than 2) bits having a common address in the test pattern and in the generated code data cover all patterns of N-bit combinations in accordance with the test pattern.

~~wherein the ECC unit generates the code information so that an arbitrary N (N is a natural number equal to or greater than 2) bits of the same address in the test pattern and in the code information generated from the test pattern cover all patterns of N-bit combinations in accordance with the inputting of the test pattern.~~

Claim 12 (Currently Amended): The semiconductor device according to claim 1,

wherein the given condition is that all bits of the generated code data are "1"s, when all bits of the test pattern, other than one specified bit, are "1"s.

~~wherein the ECC unit generates the code information so that when all the bits of the test pattern other than one specified bit are "1"s, all the bits of the code information generated from the test pattern are "1"s.~~

Claim 13 (Currently Amended): The semiconductor device according to claim 2,

wherein the given condition is that all bits of the generated code data are "1"s, when all bits of the test pattern, other than one specified bit, are "1"s.

~~wherein the ECC unit generates the code information so that when all the bits of the test pattern other than one specified bit are "1"s, all the bits of the code information generated from the test pattern are "1"s.~~

Claim 14 (Currently Amended): A method of memory test which is applied to a semiconductor device including a data memory which stores data and a code memory which

stores an error checking and correcting code (ECC code) corresponding to the data, the method comprising:

generating a test pattern ~~required to test~~ configured to test bit errors of all cells in the data memory;

outputting the test pattern to the data memory;

generating, from the test pattern, code data, as the ECC code for a test, using a Hamming matrix which meets a given condition, and outputting the code data to the code memory, the ECC unit generating the code data required for checking bit errors of all cells in the code memory using the Hamming matrix and a transposed matrix of the test pattern; and

simultaneously testing bit errors of all cells in the data memory and bit errors of all cells in the code memory by reading the test pattern written in the data memory and the code data written in the code memory.

~~generating, from the test pattern, code information having an error checking function, and outputting the code information to the code memory as the ECC code; and~~

~~simultaneously testing the data memory and the code memory by reading the test pattern written in the data memory and the code information written in the code memory.~~

Claim 15 (Currently Amended): The method according to claim 14, wherein the step of simultaneously testing includes testing whether or not all bits of the code data change from "0" to "1" or "1" to "0".

~~wherein when the test is executed, it is checked whether or not all the bits of the code information change from "0" to "1" or "1" to "0".~~

Claim 16 (Currently Amended): The method according to claim 14, wherein the step of simultaneously testing includes testing whether or not an arbitrary N (N is a natural

number equal to or greater than 2) bits having a common address in the test pattern and in the generated code data cover all patterns of N-bit combinations in accordance with the test pattern.

~~wherein when the test is executed, it is checked whether or not an arbitrary N (N is a natural number equal to or greater than 2) bits of the same address in the test pattern and in the code information generated from the test pattern cover all patterns of N-bit combinations in accordance with the inputting of the test pattern.~~

Claim 17 (Currently Amended): The method according to claim 14, wherein the step of simultaneously testing includes testing whether or not all bits of the generated code data are "1"s when all bits of the test pattern, other than one specified bit, are "1"s.

~~wherein when the test is executed, it is checked whether or not all the bits of the code information generated from the test pattern are "1"s when all the bits of the test pattern other than one specified bit are "1"s.~~